High-Efficiency Power Amplifier Integrated with Antenna

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***Abstract*—Two class B GaAs field-effect transistor (FET) power amplifiers integrated with patch antennas have been designed and fabricated at 2.48 GHz. Both amplifiers are integrated with patch antennas, which serve as load and radiator. In one case, a standard patch design was used with random harmonic termination. In another case, a modified patch design was used, which allows the tuning of the second harmonic. In this case the antenna has an additional function of a filter. An increase of 7% in the power-added efficiency (PAE) and 0.5 dB in the output power was achieved through the second harmonic tuning.**

***Index Terms*—Active antenna, class B, FET, power amplifier.**

I. Introduction

PERSONAL communication systems and cellular and cordless phones require long operating times and lightweight, compact design. In wireless transmitters the output power amplifier usually consumes the largest part of the dc power. The size and weight can be reduced by reducing the heatsink and the battery size. Therefore, the power-added efficiency (PAE) must be maximized, while still using a low voltage supply and keeping the design as compact as possible.

The PAE can be improved by optimizing the load impedance at the fundamental and by optimally loading the harmonics. Traditionally the power amplifier is designed in a 50-Ω system. Then the tuning of the second harmonic is usually done by adding a short-circuited stub, which is near one quarter wavelength long at the fundamental frequency, at the output (most often at the drain bias line) [1], [2]. At lower frequencies, this stub may be too long. The chip capacitors can be used instead, however, for rejection of the second harmonic if they have a self-resonance near the second harmonic [3].

In this letter we present a class B power amplifier design using the active antenna concept [4]. In this approach, both radiating element and harmonic tuning, which are traditionally separate subcircuits, are integrated into a single compact and efficient unit. In this letter, the tuning of the second harmonic is integrated within the antenna. Another advantage of the using active antenna approach is that the frequency slightly off that of resonance can be used as the fundamental frequency. This can simplify the design for the case when the input impedance of the antenna at the resonance is too high.

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II. Antenna Design

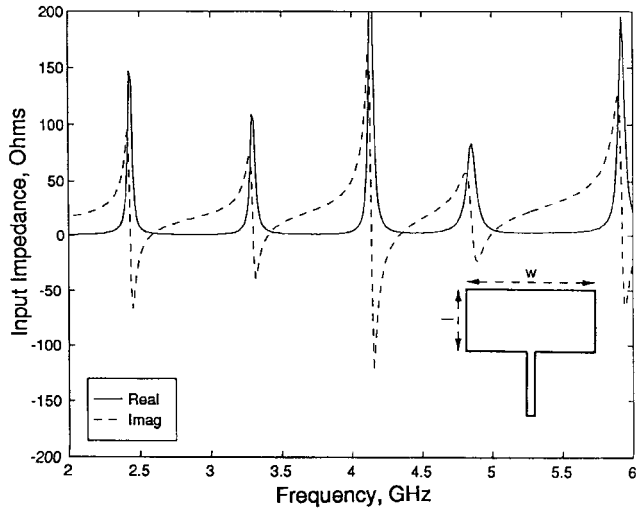
The input impedance of the antenna that would allow the second harmonic tuning should be almost zero at twice the design frequency. In this letter the patch antenna is used [6]. The input impedance of the traditional patch will not be zero at the second harmonic because of the existence of the (2,0) mode [Fig. 1(a)]. This mode exhibits an electric field that has a maximum at the middle of the patch along the nonradiating edge. At that location the electric field of the fundamental mode (1,0) is zero. Therefore, if the shorting pins are placed along that line, the (2,0) mode would be affected, while the (1,0) mode would remain unchanged. Nine shorting pins placed uniformly in the middle of the patch kill the (2,0) mode [Fig. 1(b)]. Fig. 1 shows the measured input impedance of the two patches used. Finite-difference time-domain (FDTD) code was used to verify the measured results of the input impedances, and it agreed within a few percent with the measurement.

III. Power Amplifier Design

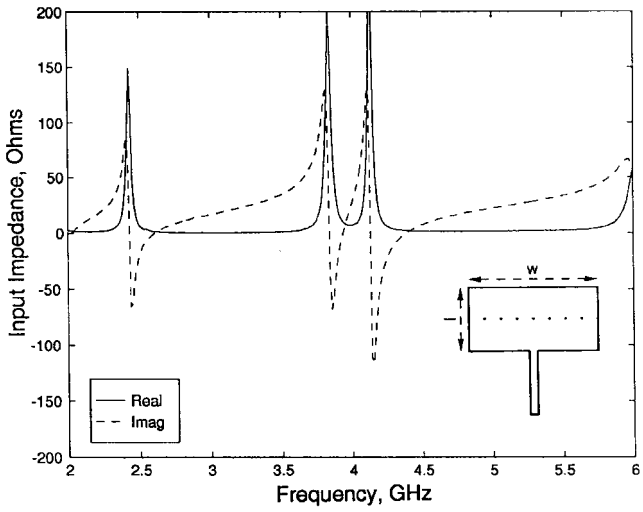
Two class B amplifiers were designed using Hewlett Packard's Microwave Design System (MDS) [5]. The device used was the Fujitsu FLL351ME power field effect transistor (FET). The large-signal model of this device (which was in the MDS's nonlinear library) and harmonic balance simulation including first three harmonics were used in the design. The drain voltage is 6 V, while the gate is biased at pinch-off. Under this bias condition, the optimum fundamental load was found to be (7-j6.5) Ω. If the patch was used at the resonance (2.43 GHz), the output matching circuit would have to provide the match from 140 Ω to (7-j6.5) Ω, which is not easy to realize. Instead, the operating frequency of 2.48 GHz was chosen at which the input impedance is (14-j30) Ω. The patch was incorporated into MDS simulation as a one-port device containing the S-parameter data from 0.13-10 GHz.

IV. Results

Two amplifiers were fabricated—one with the standard patch and another with the patch with pins. First, the gain of the patches was measured at 2.48 GHz. The measurement showed no significant difference between the regular patch and the patch with pins. The measured gain was 7.8 dB. The



(a)



(b)

Fig. 1. The measured input impedance of (a) regular and (b) modified (with pins) patch antennas with dimensions $l = 1.55$ in and $w = 2.32$ in, using HP Network Analyzer. In case (b) nine shorting pins are uniformly located in the middle of the l dimensions.

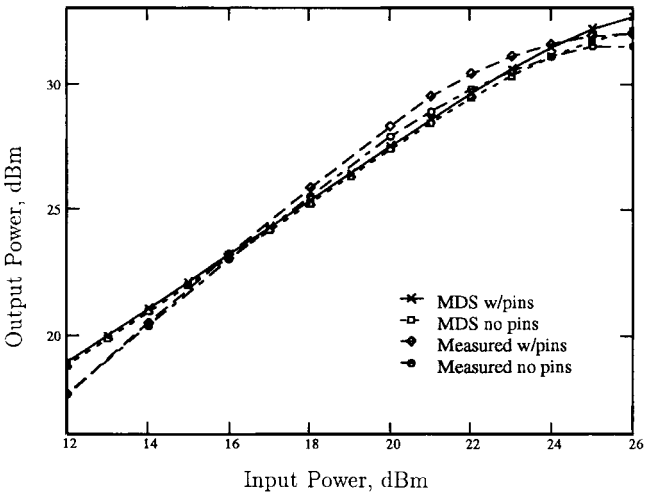


Fig. 2. Measured and theoretical (MDS) output power versus the input power for two amplifiers: "w/pins" means that the second harmonic is tuned through the antenna; "no pins" means that the second harmonic has random termination.

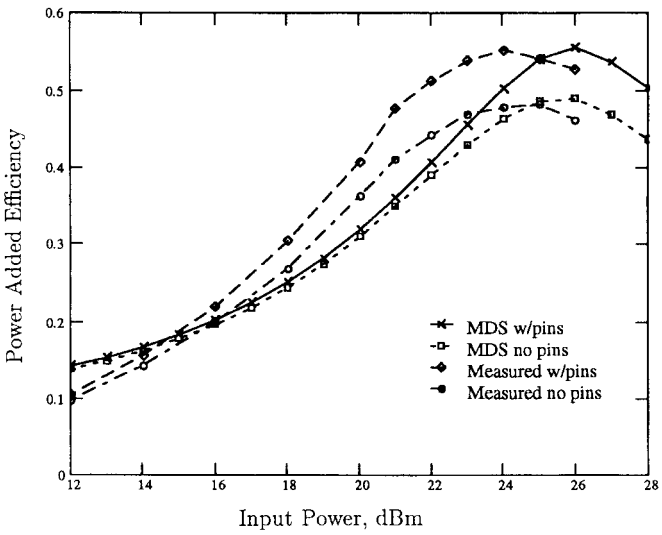


Fig. 3. Measured and theoretical (MDS) PAE versus the input power for two amplifiers: "w/pins" means that the second harmonic is tuned through the antenna; "no pins" means that the second harmonic has random termination.

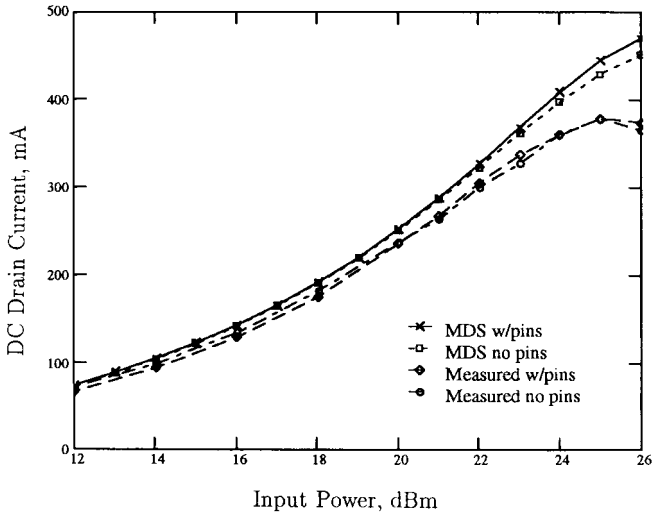


Fig. 4. Measured and theoretical (MDS) dc drain current versus the input power for two amplifiers. "w/pins" means that the second harmonic is tuned through the antenna; "no pins" means that the second harmonic has random termination.

directivity of the patch with pins was calculated using the FDTD method and was found to be 7.9 dB, which showed close agreement with the measured result.

The output power of the amplifiers with integrated patches was measured in an anechoic chamber using the Friis free-space equation [6]. The receiver used was a broadband horn antenna with 7.5 dB gain at 2.48 GHz. The results are shown in Figs. 2–4. The output power and the PAE in Figs. 2 and 3 were calculated based on the amplifier power only (and do not include the patch antenna gain). MDS predicted about 0.5-dB increase in the P1dB due to the second harmonic termination, while the measurement showed the increase of the output power at the maximum efficiency of about 0.5 dB. Since there is always an error associated with the measurement of the radiated power from an active antenna, the 0.5-dB result represents the minimum difference in the output power

between the two amplifiers when exactly the same setup is used. The PAE is increased by 7% when the patch with pins is used, which is close to the theoretical prediction of 6.6%. The maximum measured PAE is 55% at the output power of 31.6 dBm for the amplifier with the harmonic tuning. Fig. 4 shows the increase in the average dc drain current due to the self-biasing in class B operation.

V. Conclusion

Two class B GaAs FET power amplifiers were developed. Both utilize the active antenna concept with patch antennas as the radiating elements. One amplifier uses the standard patch, while another uses the modified patch in which the termination of the second harmonic is almost zero. The tuning of the second harmonic increased the power added efficiency by 7% and the output power by 0.5 dB.

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